USB 3.0 ENGINEERING CHANGE NOTICE

ECN# 011

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USB 3.0 ENGINEERING CHANGE NOTICE

Title: USB3.0 Peripheral USPort State Machines ECR

Applied to: USB3.0 (11132008)-final

Brief description of the functional changes proposed:
Updated US port state machine to increase robustness of SS link. Made changes to US port state machine and Link chapter to bring them into synch with each other.

Benefits as a result of the proposed changes:
Makes the SS link more robust in the light of the introduction of the “Disabled.Error” state.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
No changes to current devices, SS peripheral devices that conform to the new specification will have a lower probability of being forced to USB2 mode permanently due to typical system events.

An analysis of the hardware implications:
Applies to all USB3 devices, including OTG.

An analysis of the software implications:
Applies to all USB3 devices, including OTG.

An analysis of the compliance testing implications:
Compliance tests need to test new behavior with respect to the Disabled.Error state.

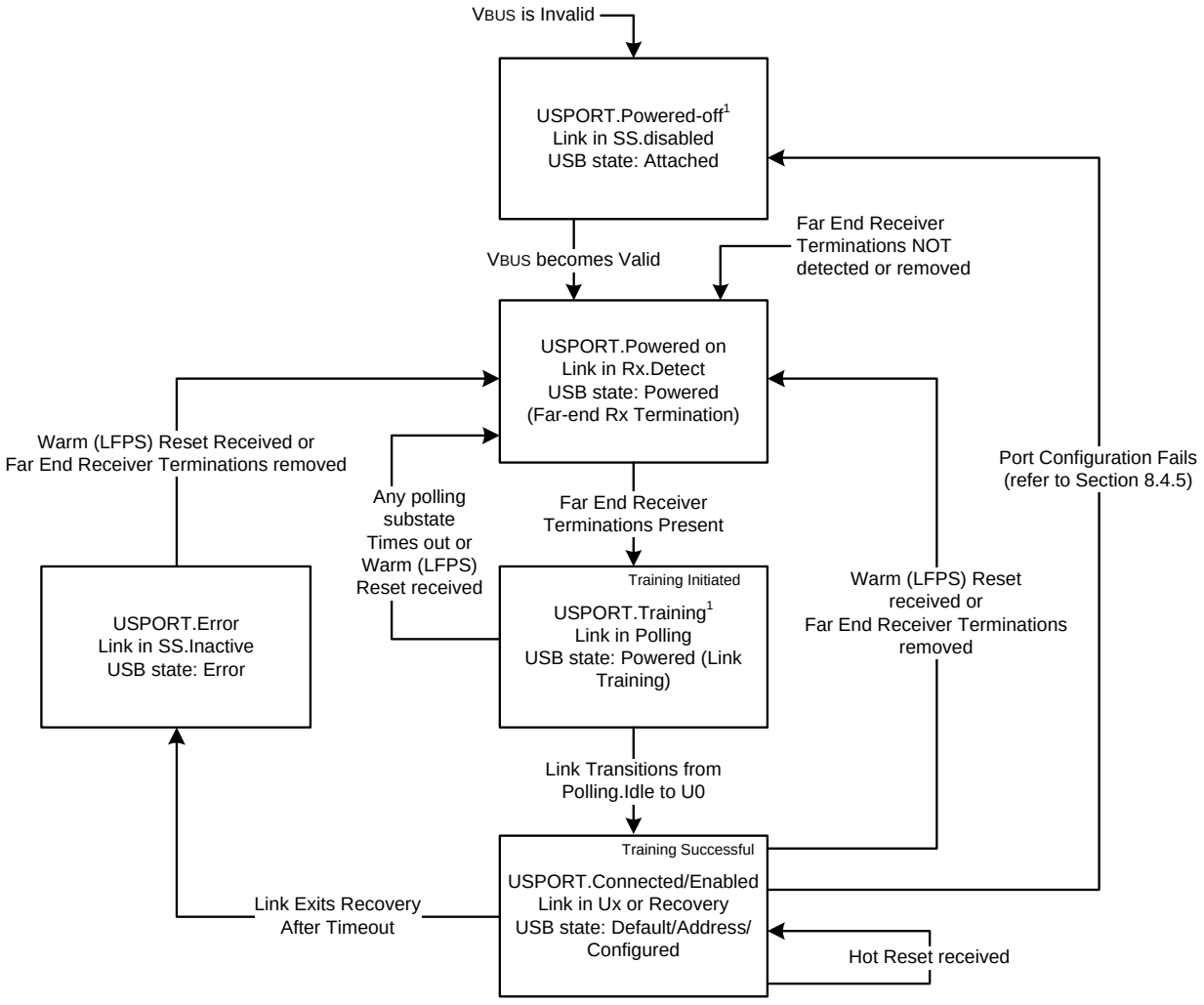
Actual Change Requested

(a). Amendments proposed to Section 10.5 (Figure 10- 11)

Replace current Figure 10-11 in Section 10.5 with the figure below:

Made a change to bring the state machine in sync with the LTSSM description in chapter 7 (and figure 7-16).

- Updated the Arc from USPort.training to USPort.powered-on to include “warm(LFPS) reset”.



[1] If Port Configuration fails, the port shall transition to the USPORT.Powered-off state with the link in SS.Disabled state and USB Device in the Attached state. Vbus may still present on the upstream port. Vbus must be toggled to transition to the USPORT.Powered on state.

Changes to the text for Section 10.5 are redlined below:

10.5.1.2 USPORT.Powered-on

A port shall transition into this state in any of the following situations:

- From the USPORT.Powered-off state when VBUS becomes valid.
- From the USPORT.Error state when the link receives a warm reset or if Far-end Terminations are removed.
- From the USPORT.Connected/Enabled state when the link receives a Warm Reset.
- From the USPORT.Training state if the port's link times out from any Polling substate OR if the port receives a Warm (LFPS) Reset.

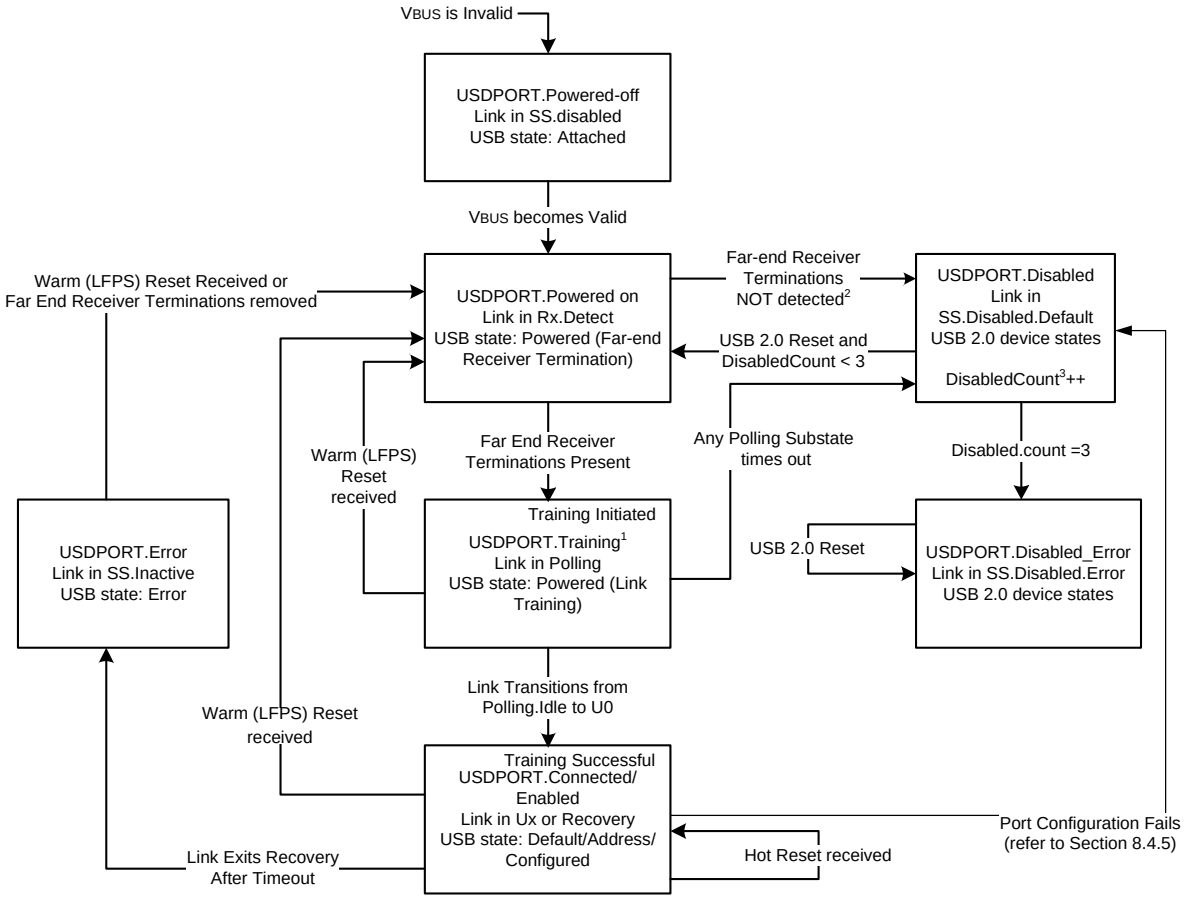
(b). Amendments proposed to Section 10.16.2 (Figure 10-25)

Changes to the Upstream Port State Machine:

- Added arc from USDPort.Training to the USDPort.Powered On state to make this state machine consistent with the LTSSM Polling Substate Machine (figure 7- 16).
- Made changes corresponding to the changes in the text in sections 10.16.2.6 and 10.16.2.7

10.16.2 Peripheral Device Upstream Port State Machine

The following sections provide a functional description of a state machine that exhibits correct peripheral device behavior for when to connect on SuperSpeed or USB 2.0. Figure 10-25 is an illustration of the peripheral device upstream port state machine.



[1] Peripheral Device must disconnect on USB2.0 within tUSB2SwitchDisconnect of entering this state

[2] If USPORT.Powered on was entered from any state except USPORT.Disabled then this transition shall take place if Far-end Receiver Terminations (RRX-DC) are not detected after 8 successive Rx.Detect.Quiet to Rx.Detect.Active transitions. If USPORT.Powered on was entered from the USPORT.Disabled state, then this transition shall take place the first time that Far-end Receiver Terminations are not detected in the Rx.Detect.Active substate.

[3] Disabled count is incremented each time the "Disabled" state is entered. Disabled count is reset to '0' each time the link completes Port Configuration.

Figure 10-15. Peripheral Upstream Device Port State Machine

10.16.2.6 USDPORT.Disabled

A port transitions to this state

- From the USDPORT.Powered on state when Far-end Receiver Terminations are not detected as per the rules described below:

  If USDPORT.Powered on was entered from any state except USDPORT.Disabled then this transition shall take place if Far-end Receiver Terminations (RRX-DC) are not detected after 8 successive Rx.Detect.Quiet to Rx.Detect.Active transitions.

  If USDPORT.Powered on was entered from the USDPORT.Disabled state, then this transition shall take place the first time that Far-end Receiver Terminations are not detected in the Rx.Detect.Active substate.

- From the USDPort.Training state if a timeout occurs on any Polling substate (see fig. 7-16).
- From the USDPort.Connected state, if the Port Configuration process times out (see section 8.4.5).

A count (*Disabled_count*) shall be maintained of each entry into the USDPort.Disabled state.

- Count is initialized to ‘0’ upon power on reset.
- The count is incremented upon each entry into the USDPort.Disabled state (i.e., each increment is the result of one entry into the USDPort.Disabled state).
  - If the count equals 3 the port transitions to the Disabled.Error state.
- The count is reset to ‘0’ upon a successful completion of the Port Configuration process.

In this state, the port's link shall be in the SS.Disabled state. The corresponding peripheral device USB state shall USB2.0 Device States.

10.16.2.7 USDPORT.Disabled_Error

A port transitions to this state from the USDPort.Disabled state when *Disabled_Count = 3.*

- The port shall remain in USDPORT.Disabled_Error state if the port’s link receives a USB2.0 reset.

In this state, a fatal error has been detected on the port's link and the link shall be in the SS.Disabled state. The corresponding peripheral device USB state shall be USB2.0 Device States.

(c). Amendment proposed to Section 7.5.1

Make the following changes:

7.5.1 SS.Disabled

SS.Disabled is a state with a port’s low-impedance receiver termination removed. It is a state where a port’s SuperSpeed connectivity is disabled. Refer to Section 10.16 for details regarding the behavior of a peripheral device. Refer to Sections 10.3 to 10.6 for behaviors regarding a hub’s upstream port and downstream port.
SS.Disabled does not contain any substates in the case of downstream ports and hub upstream ports. For a peripheral upstream port, it contains two substates, SS.Disabled.Default and SS.Disabled.Error.
SS.Disabled is also a logical power-off state for a self-powered hub upstream port.

SS.Disabled.Default is also a logical power-off state for a self-powered peripheral upstream port.
A downstream port shall transition to this state from any other state when directed.
A self-powered hub or peripheral upstream port shall transition to this state when V_{BUS} is not valid.

7.5.1.1 SS.Disabled for Downstream Ports and Hub Upstream Ports

SS.Disabled for Downstream Ports and Hub Upstream Ports does not contain any substates.

7.5.1.1.1 SS.Disabled Requirements

• V_{BUS} may be present during SS.Disabled.
• The port's receiver termination shall present high impedance to ground of $Z_{RX-HIGH-IMP-DC-POS}$ defined in Table 6-13.
• The port shall be disabled from transmitting and receiving LFPS and SuperSpeed signals.

7.5.1.1.2 Exit from SS.Disabled

• A downstream port shall transition to Rx.Detect when directed.
• An upstream port shall transition to Rx.Detect only when V_{BUS} transitions to valid or a USB 2.0 bus reset is detected.

7.5.1.2 SS.Disabled for Upstream Ports of Peripheral Devices

SS.Disabled of a peripheral device operates similarly to hub upstream ports, except that it only attempts a limited number of SuperSpeed attempts upon USB2.0 bus reset.

7.5.1.2.1 SS.Disabled Substate Machine

SS.Disabled of a peripheral device has two substates shown in Figure 7-14.

- SS.Disabled.Default
- SS.Disabled.Error

SS.Disable.Default is a logical power-off state for a self-powered peripheral device.

7.5.1.2.2 SS.Disabled Requirements

The requirements of a peripheral upstream port are the same as defined in Section 7.5.1.1.1. In addition, a peripheral upstream port shall implement a tDisabledCount counter. The operation of the tDisabledCount counter shall meet the following requirement.

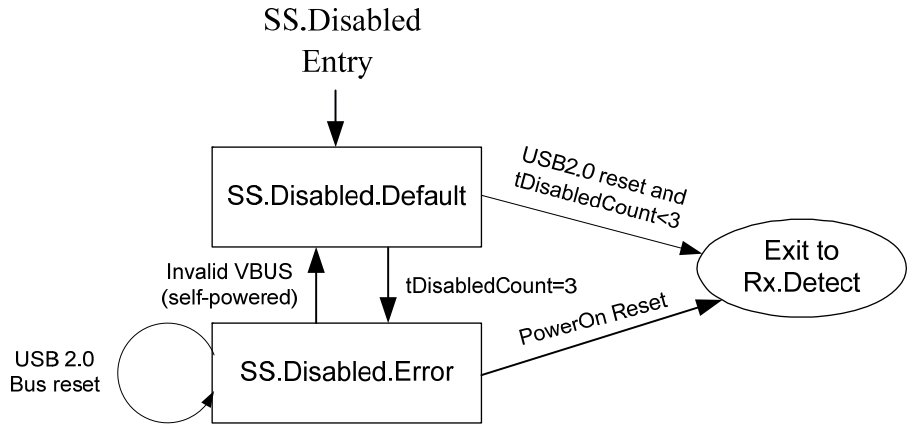
- The tDisabledCount counter shall be reset to zero upon one of the following two conditions.
    1. Invalid VBUS
    2. Successful port configuration exchange
- The tDisabledCount counter shall be incremented upon entry to SS.Disabled.Default.

7.5.1.2.3 Exit from SS.Disabled.Default

- A peripheral upstream port shall transition to Rx.Detect if one of the following conditions are met.
    1. When VBUS transitions to valid.
    2. When a USB2.0 bus reset is detected and tDisabledCount is less than 3.
- A peripheral upstream port shall transition to SS.Disabled.Error if tDisabledCount is 3.

7.5.1.2.4 Exit from SS.Disabled.Error

- A peripheral upstream port shall transition to Rx.Detect upon PowerOn reset.
- A self-powered peripheral upstream port shall transition to SS.Disabled.Default upon detection of invalid VBUS.
- A peripheral upstream port shall remain in SS.Disabled.Error upon detection of USB 2.0 bus reset.



Note: Transition conditions are illustrative only.